synertronixx GmbH, 2007-11-02

Embedded Socket Computer

SCB9520

Embedded Socket Computer SCB9520

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1 Introduction

The Embedded Socket Computer SCB9520 is a small "Computer-On-Module" board designed to serve as a building block in embedded applications. The SCB9520 is based on a 520MHz Marvell/Intel industrial-standard PXA270 controller with 64 KBytes cache. It's standard JEDEC DIL-64 format modul makes it fast, extremely easy and affordable to add remote device management capabilities to electronic devices. The SCB9520 has all the components required to run operating systems such as Linux and Windows CE.

The rich feature set of the Embedded Socket Computer SCB9520 combines a 32-bit CPU, SDRAM, Flash Disk and vital computing peripherals. For embedded applications, the SCB9520 provides a 100Mbit Ethernet, USB, I^2C serial ports and many other essential functions.

The CPU is based on the ARM™ RISC technology. In a standard application with 100 MBit ethernet enabled the total power consumption is 1.2W typ. No fans or heatsinks are required which results in high reliability and zero noise. The Embedded Socket Computer SCB9520 is specially designed for high performance ethernet and memory intensive applications, requiring high network throughput rates on embedded computer modules. Typical applications include industrial automation systems, point-of-sale, data acquisition, building automation and control systems.

The SCB9520 is preinstalled with an uboot 1.2.0 bootloader, an embedded LINUX 2.6.20, a busy box and a preconfigured network interface. It is designed as a drop-in microcontroller replacement and contains the microprocessor core, the ethernet controller 32 MByte NOR Flash, a 2GByte Flash Disk and up to 128 MByte

Low-Power SDRAM. The modular approach in conjunction with a full featured LINUX offers significant advantages compared to full custom designs since it cuts down development times from month or years to days or weeks and shielding complex board technology from the user; e.g. fine pitch and multilayer PCBs, BGA assembly and porting operating systems.

The following capabilities are supported by the SCB9520:

- **Network Protocols**
  ARP, IPV4, ICMP, UDP, TCP, HTTP, DHCP, TFTP, FTP, POP3, SMTP, SCP
- **Network Interface**
  10/100Mbit IEEE 802.3 Ethernet interface
  On-board magnetics
  Pre-programmed MAC-address
- **Device Interface**
  2 serial ports
  1 I²C interface
  2 USB interfaces (host and device) support
  16-bit data and 18-bit address bus

2 SCB9520 Features

- Marvell/Intel® PXA270 32-bit Xscale CPU
- 520MHz Clock Speed
- Realtime Linux 2.6.20 preinstalled
- 32-bit SDRAM (64, 128 MBytes)
- NAND Flash Disk (1G, 2G)
- NOR Flash Memory (32 MByte)
- 10/100 MBit/s fast ethernet controller
- One Low/Full speed USB 1.1 host controller
- One Low/Full speed USB 1.1 device controller
- Two high-speed UARTs (up to 921.6 kBd)
- I^2C-Interface (up to 400 kHz clock)
- Memory management unit (MMU)
- Integrated realtime clock
- On-board reset controller
- Programmable watchdog timer
- Two independent chip selects
- External 16-bit bus interface
- 64-pin JEDEC DIL connector
- JTAG IEEE 1149.1 debug interface
- 3.3V low power design (± 5%)
- Supply current 360mA typ @520MHz
- Size 83 x 27 mm

3 Embedded Software

- Embedded Linux 2.6.20
- Bootloader uboot 1.2.0
- Board support for Marvell/Intel® PXA270 CPU
- DM 9000 ethernet packet driver
- Driver support for UART, I^2C and GPIO
- Driver support for USB host
- NAND / NOR Journaling flash file driver JFFS2
- TCP/IP stack
- Integrated HTTP and FTP-server

4 PXA270 Processor

The Marvell/Intel® PXA270 CPU is high-performance 32-bit RISC Xscale core running at 520 MHz, while system speed is running at 104 MHz. The PXA270 incorporates the Intel XScale® technology which complies with the ARM v5TE instruction set (excluding floating-point instructions) and follows the ARM programmer's model. The PXA270 processor also provides Intel® Wireless MMX™ media enhancement technology, which supports integer instructions to accelerate audio and video processing.

In addition, it incorporates Wireless Intel Speedstep® Technology, which provides sophisticated power management capabilities enabling excellent MIPs / mW performance. Its internal bus architecture and fast system speed provides an outstandig performance which is an ideal solution for network and wireless applications.

The PXA270 processor is an integrated system-on-a-chip microprocessor for high performance, dynamic, low-power portable handheld and hand-set devices. It provides a scalable, bi-directional data interface, supporting seven logical channels and other features. The operating-system (OS) timer channels also accept an external clock input.

The processor memory interface gives designers flexibility as it supports a variety of external memory types. The processor also provides four 64 kilobyte banks of on-chip SRAM, which can be used for program code or multimedia data. Each bank can be configured independently to retain its contents when the processor enters a low-power mode.

The PXA270 processor provides industry-leading multimedia performance, low-power capabilities and rich peripheral integration. A set of serial devices and general-system resources offers computational and connectivity capability for a variety of applications.

Two 32 kByte caches are implemented, one for instructions, the other for data. A 32-bit data bus connects each cache to the XScale 270 core allowing a 32-bit instruction to be fetched and fed into the instruction decode stage of the pipeline at the same time as a 32-bit data access for the Memory stage of the pipeline.

The main important features of the PXA270 are:

- 520 MHz processing speed
- 104 MHz external bus clock
- 32K instruction cache and 32K data cache
- XScale high performance 32-bit RISC engine
- Thumb® 16-bit compressed instruction set for a leading level of code density
- EmbeddedICE™ JTAG software debug
- user code binary compatibility with ARM7TDMI® and StrongARM processors

5 Memory

The Embedded Socket Computer SCB9520 is assembled with up to 128 MByte of SDRAM, 32 MByte of fast access NOR Flash and up to 2GBytes NAND Flash. The memory interface is designed for fast start-up times and high throughput rates. The system speed of the memory is 104 MHz. Customer variations of the memory size can be assembled on request.

The XScale core uses a flat memory model. All internal as well as the external peripherals are mapped into the 4 GBytes address spaces of the PXA270 CPU.

DRAM

The SCB9520 can be assembled with 64 or 128 MBytes of Synchronous DRAM. The SDRAM interface is 32-bits wide and runs at a 104 MHz clock.

NOR Flash

The SCB9520 is assembled with 32 MBytes of linear NOR Flash ROM. The first 256 kBytes are used for uboot (bootloader) and e, the remainder is used for O/S Kernel and Flash Disk implementation.

NAND Flash

One of the key advantages of the Embedded Socket Computer SCB9520 is its on-board flash disk for applications requiring large, non-volatile on-board storage. The Flash Disk behaves exactly like a regular hard disk drive; however, it doesn't have any moving parts and it is built into the SCB9520 module.

The NAND Flash is a block device – optimized for block read and write operations rather than for random access. The NAND Flash is available in sizes of 1 and 2 GBytes. The Embedded Socket Computer SCB9520 is designed for upward compatibility with future NAND Flash devices of larger capacity.

The Flash Disk is implemented by three parts:

- Flash memory component - NOR and NAND
- Interface logic
- Flash Disk Driver firmware

wear leveling

The Flash Disk Driver ensures that block write operations will be distributed evenly across the physical media, regardless of the location (logical sector number) requested by the operating system. Even distribution ensures that all Flash blocks will be worn at the same (slow) rate and the Flash will continue operating for a long time without reliability degradation.

6 Block Diagramm

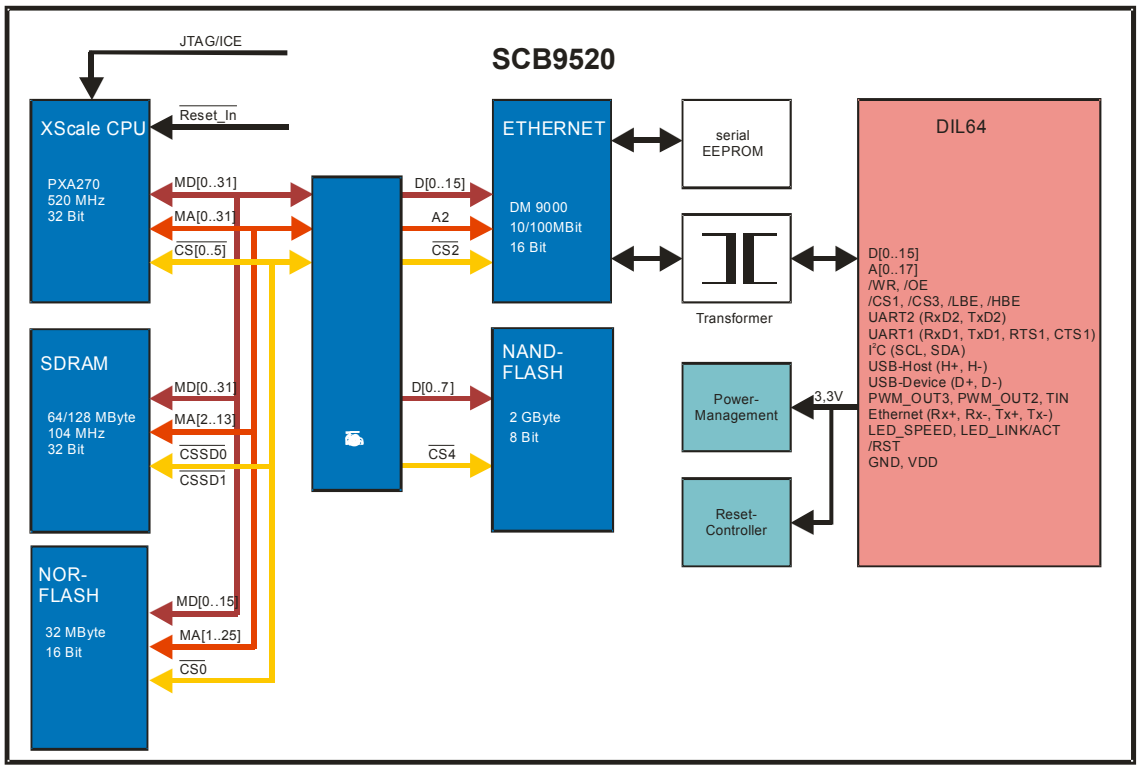

Figure 1: Block Diagramm

7 Ethernet Interface

The SCB9520 contains one full-featured 10/100 Mbit Ethernet interface, which is fully compatible with the IEEE802.3 standard. The Ethernet interface is based on the Davicom DM9000 component. The DM9000 consists of both a Media Access Controller (MAC) and a physical layer (PHY) combined into a single component solution. On chip features are a 8 kByte internal transmit and receive FIFO and a quasi DMA interface to the processor bus (sequential write/read access). The Davicom DM9000 communicates with the PXA270 processor on a 16-bit local bus.

The DM9000 ethernet controller can operate in either full duplex or half duplex mode. In full duplex mode, it adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a collision reduction mechanism. The DM9000 includes a PHY interface to the wire transformer at rates of 10BASE-T and 100BASE-TX, and Auto-Negotiation capability for speed, duplex and flow control.

The CSMA/CD unit of the DM9000 allows it to be connected to either a 10 or 100 Mbit/s Ethernet network. The CSMA/CD unit performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc.

The CSMA/CD unit can also be placed in full-duplex mode allowing simultaneous transmission and reception of frames. The Physical Layer (PHY) unit of the DM9000 allows connection to either a 10 or 100 Mbit/s Ethernet network. The PHY unit supports Auto-Negotiation for 100BASE-TX Full Duplex, 100BASE-TX Half Duplex, 10BASE-T Full Duplex and 10BASE-T Half Duplex.

The SCB9520 also supports LED pins to indicate link status, and speed. DM9000 initialization parameters, including MAC Address, are stored in an serial EEPROM and uploaded into the ethernet controller on power-up. As the SCB9520 contains on-board magnetics for ethernet connectivity no external components are required.

8 UARTs

The 2 UARTs of the Socket Computer SCB9520 provides serial communication capability with external devices through an LV-CMOS UART. Each serial port contains also a slow infrared-transmit encoder and receive decoder that conform to the IrDA serial-infrared specification. The processor can read a UART's complete status during functional operation. Status information includes the type and condition of transfer operations and error conditions (parity, overrun, framing, or break interrupt) associated with the UART.

Each serial port operates in either FIFO or non-FIFO mode. In FIFO mode, a 64-byte transmit FIFO holds data from the processor until it is transmitted on the serial link, and a 64-byte receive FIFO buffers data from the serial link until it is read by the processor. In non-FIFO mode, the transmit and receive FIFOs are bypassed. Each UART includes a programmable baud-rate generator that can divide the input clock by 1 to (216 – 1). This produces a 16X clock that can be used to drive the internal transmit and receive logic. Software can program interrupts to meet its requirements, which minimizes the number of computations required to handle the communications link. Each UART operates in an environment that is either controlled by software and can be polled or is interrupt-driven.

Both UARTs support the 16550A and 16750 functions, but are slightly different in the features supported. The UART1 (equivalent to the PXA270 BTUART) is a high-speed UART that supports baud rates up to 921.6 kBd and can be connected to a Bluetooth module. It supports two modem control pins (/CTS and /RTS).

The UART2 (equivalent to the PXA270 STUART) does not support modem control capability. The maximum baud rate is 921.6 kBd

The UART pins are not 5V tolerant.

9 I²C

I²C is a two-wire bidirectional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection between devices. The flexible I²C bus allows additional devices to be connected to the bus for expansion and system development. The I²C can be configured as master or slave. Multi-master configurations are supported by featuring collision and arbitration detection to prevent data corruption.

The I²C interface uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. For I²C compliance, all devices connected to these two signals must have open drain or open collector outputs with an additional pull-up resistor. The I²C interface only supports 3.3V devices. The clock rate is selectable to 100kHz or 400kHz.

The SCL and SDA pins are not 5V tolerant.

10 USB

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals can be attached, configured, used, and detached, while the host and other peripherals continue operation.

USB Host Controller

The Socket Computer SCB9520 can contain one or two host USB ports. The interface of one USB host port of PXA270 is shared with slave port, and is configured by default as slave. These USB ports are Open Host Controller Interface (Open-HCI) compliant. The Open-HCI specification provides a register level description for a host controller, as well as common industry hardware / software interface and drivers, including keyboard and mouse support.

Features

- One or two host USB ports, depending on host / slave selection.
- 12 Mbps or 1.5 Mbps speed
- Fully compatible with USB specification version 1.1 and OHCI 1.0 register model

Since the USB Host Ports conform to OHCI standard, the description of their operation is not provided in this manual. For more information refer to the Universal Serial Bus Specification, Revision 1.1, the On-The-Go Supplement to Universal Serial Bus Specification, Revision 2.02, and the Pull-up / Pull-down Resistors

Engineering Change Notice to the USB 2.0 Specification3 for a full description of the USB protocol and its operation.

A USB host must supply 5.0 volts (per the USB specification); however, the SCB9520 does not have 5Volt tolerant pads.

USB Device Controller

The USB Device Controller is contained in the PXA270 processor chip. The Universal Serial Bus device controller (UDC) is Revision 1.1-compliant, full-speed device that operates half-duplex at a baud rate of 12 Mbps and supports all standard device requests issued by any USB host controller. The UDC supports 24 endpoints (endpoint 0 plus 23 programmable endpoints).

The UDC uses single-ported memory to support FIFO operations. Bulk, isochronous, and interrupt endpoint FIFO structures can be double-buffered to enable the endpoint to process one packet while assembling another. Either DMA or the software loop can be used to fill and empty the FIFOs. An interrupt, DMA service request, or polling can be used to detect packet receipt.

Features:

- USB Revision 1.1, full-speed compliant device
- 23 programmable endpoints

  - Type: bulk, isochronous, or interrupt

  - Direction: in or out

  - Maximum packet size

  - Programmable configuration, interface and alternate interface setting numbers
- Endpoint 0 for control IN and OUT
- Four configurations:

  - Three programmable configurations with up to seven interfaces with seven alternate interface settings

  - Default configuration 0 with one interface and control endpoint 0
- Configurable 4-KByte memory for endpoint data storage

The UDC consists of four major components: the peripheral bus interface, endpoint memory, endpoint control, and USB interface.

The peripheral bus interface contains the UDC control and status registers for the endpoint configuration data and provides the interface between the PXA270 processor and the USB data. The endpoint memory is a 4 KByte SRAM used for USB endpoint data storage. It has 32 bytes dedicated to endpoint 0, allowing the remainder of its memory to be allocated to any of the 23 programmable endpoints. The endpoint control and USB interface blocks provide the USB functionality.

For more information refer to the Universal Serial Bus Specification, Revision 1.1, and the On-The-Go Supplement to Universal Serial Bus Specification, Revision 2.0 for a full description of the USB protocol and its operation.

11 Operating System Timers

The operating system timers block provides a set of timer channels that allows software to generate timed interrupts (or wake-up events). In the PXA270 processor, these interrupts are generated by two sets of timer channels. The first set, which provides one counter and four match registers, is clocked from a 3.25 MHz clock. The other set, which provides eight counters and eight match registers, can be clocked from either the 32.768 kHz timer clock, a 13 MHz clock, or an externally supplied clock, providing a wide range of timer resolutions.

The first set of timers provide the following features:

- Single counter operating at 3.25 MHz
- Four Match registers
- Watchdog function.

The second set of timers provides an independent clock source for each counter, selectable by software:

- 32.768 kHz clock for low power
- 13 MHz clock for high accuracy
- Externally-supplied clock for network synchronization
- Counter resolutions of 1/32768th of a second, 1 millisecond, 1 second, and 1 microsecond
- Periodic and one-shot timers
- Two external synchronization events
- Operation during reduced-power modes (standby, sleep, and deep-sleep modes)

12 External Peripheral Bus

An 8/16-bit data bus and a 18-bit address bus are provided for connecting external peripherals to the SCB9520. Any external bus pin is LV-CMOS compatible. Two individually programmable chip selects (/CE1, /CE3) and a /RD and /WR signal allow using a wide range of 8- and 16-bit peripherals to be connected directly to the SCB9520. Each chip select has programmable access time settings which allows mixing fast and slow peripherals on the same databus. By using the /LBE and /HBE signals external memory can accessed byte wide.

In order to reduce the bus loads of the PXA270 processor, the Socket Computer SCB9520 provides an internal System Memory Bridge, which decouples the

internal bus traffic to the external peripherals. This leads also to a reduced EMI, as fast switching signals

The external peripheral bus is not 5V tolerant.

13 Hardware Reset

A power-on reset generator (POR) with low voltage detection resets all components on the the module. An external reset signal can be used to reset the processor core. The reset generator trips at 2.93V and generates an internal 500ms reset signal. If an external reset signal is applied to the /RES input pin, this signal is stretched by 100ms in order to prevent signal bouncing.

During hardware reset, the following conditions occur:

- All internal registers and processes are held at their defined reset conditions.
- While reset is asserted, the only activity inside the processor is the stabilization of the 13-MHz processor oscillator and phase-locked loops.
- The remaining internal clocks are stopped and the chip is fully static.
- All pins assume their reset conditions.

The reset input pin is not 5V tolerant.

14 Bootloader

The SCB9520 is shipped with a preinstalled bootloader uboot 1.2.0. The bootloader can be disabled in order to start immediately the operating system. Only a simple PC terminal program is necessary to work with the bootloader. Downloads can performed over the serial interface or ethernet. The uboot bootloader uses a TFTP server for downloading programs. The download option over ethernet results in highly reduced download and update times.

15 Linux

The SCB9520 contains a preinstalled, full featured and performance optimised LINUX (kernel version 2.6.20) operating system with TCP/IP, embedded Web server, FTP server, Telnet server and journaling flash file system support. The embedded LINUX contains all necessary drivers for controlling the UART, ethernet, USB host, I^2C and the GPIO ports.

16 Flash Memory Partitions

NOR and NAND are two different technologies of Flash components. NOR technology has capabilities and a price advantage in low capacities while NAND technology has faster write speeds and price advantages in higher capacities. The SCB9520 has one NOR and one NAND flash on-board. The NOR flash memory of SCB9520 contains 32 MBytes of Fast Sync Burst Memory and up to 2 GBytes of NAND flash. The NOR Flash is divided into 4 partitions while the NAND flash has only one partition and uses a flat memory model for data storage.

The following table 1 show the usage of the NOR flash file system:

Table 1: NOR Flash Memory Partitions

Physical Address	Description	Size
0x0000 0000 **0x0001 FFFF**	Bootloader u-boot 1.2.0	128 kByte
0x0002 0000 **0x0003 FFFF**	u-boot Environment	128 kBytes
0x0004 0000 - **0x0023 FFFF**	LINUX 2.6.20 kernel	2 MByte
0x0024 0000 - **0x01FF FFFF**	Root File System	29.75 MBytes

17 Memory Map

Table 2: Physical Memory Map

Physical Address	Description	Chip-Select PXA270	Size
0x0000 0000 - 0x03FF FFFF	Boot NOR Flash	/CS0	64 MBytes
0x0400 0000 - 0x0403 FFFF	External /CS1	/CS1	256 kBytes
0x0404 0000 - 0x07FF FFFF	Do not use	n.a.	63.75 MBytes
0x0800 0000 - 0x0800 FFFF	DM 9000	/CS2	64 kBytes
0x0801 0000 - 0x0BFF FFFF	Reserved	n.a.	63.9 MBytes
0x0C00 0000 - 0x0C03 FFFF	External /CS3	/CS3	256 kBytes
0x0C04 0000 - 0x0FFF FFFF	Do not use	n.a.	63.75 MBytes
0x1000 0000 - 0x13FF FFF	NAND Flash Disk	/CS4	64 MBytes
0x1400 0000 - 0x17FF FFFF	Reserved for future use	/CS5	64 MBytes
0x1800 0000 - 0x1FFF FFFF	Reserved	n.a.	128 MBytes
0x2000 0000 - 0x2FFF FFFF	Compact Flash Slot 0 (not used)	n.a.	256 MBytes
0x3000 0000 - 0x3FFF FFFF	Compact Flash Slot 1 (not used)	n.a.	256 MBytes
0x4000 0000 - 0x43FF FFFF	Peripherals memory-mapped registers	n.a.	64 MBytes
0x4400 0000 - 0x47FF FFFF	LCD memory-mapped registers (not used)	n.a.	64 MBytes
0x4800 0000 - 0x4BFF FFFF	Memory controller registers	n.a.	64 MBytes
0x4C00 0000 - 0x4FFF FFFF	USB host memory-mapped registers	n.a.	64 MBytes
0x5000 0000 - 0x53FF FFFF	Capture interface registers (not used)	n.a.	64 MBytes
0x5400 0000 - 0x57FF FFFF	Reserved	n.a.	64 MBytes
0x5800 0000 - 0x5BFF FFFF	Internal memory control	n.a.	64 MBytes
0x5C00 0000 - 0x5C03 FFFF	Internal SRAM	n.a.	256 kBytes

Table 3: Physical Memory Map

Physical Address	Description	Chip-Select PXA270	Size
0x5C04 0000 - 0x5FFF FFFF	Reserved	n.a.	63.75 MBytes
0x6000 0000 - 0x7FFF FFFF	Reserved	n.a.	512 MBytes
0x8000 0000 - 0x9FFF FFFF	Reserved	n.a.	512 MBytes
0xA000 0000 - 0xA3FF FFFF	SDRAM Partition 0	/SDCS0	64 MBytes
0xA4000 0000 - 0xA7FF FFFF	SDRAM Partition 1	/SDCS1	64 MBytes
0xA800 0000 - 0xABFF FFFF	SDRAM Partition 2 (reserved for future use)	/SDCS2	64 MBytes
0xAC00 0000 - 0xAFFF FFFF	SDRAM Partition 3 (reserved for future use)	/SDCS3	64 MBytes
0xB000 0000 - 0xFFFF FFFF	Reserved	n.a.	1.25 GBytes

18 Pin Descriptions

Table 4: Description of Pin Numbers and its function

Pin Group	Pin Name	Pin Number	Direction	Function
CPU Bus	D0-D7 D8-D15	31-24 33-40	I/O	Bidirectional Data bus. The Data bus D0-D15 is connected through the system memory bridge to the PXA270
	A0-A17	23-6	Out	Address bus. The Address bus is buffered by the system memory bridge.
	/RD	2	Out	Read Enabe. Pin is connected through the system memory bridge to the /OE-Pin of the PXA270. Read enable is low active.
	/WR	3	Out	Write Enable. Pin is connected through the system memory bridge to the /OE-Pin of the PXA270. Write Enable is low active.
	/CS1 /CS3	5 4	Out Out	Chip Select. Pins are connected through the system memory bridge to the /CS1 and /CS3-Pins of the PXA270
	/LBE /HBE	44 43	Out	Byte enable. /LBE is the strobe signal for D[0..7], /HBE is the strobe signal for D[8..15].
Power	/RES	57	In	Master reset input. Internal 15k Pullup.
	GND	32	Power	Ground
	VDD	64	Power	Positive Power Supply

Table 5: Pin configuration of the Ethernet and USB interface

Pin Group	Pin Name	Pin Number	Direction	Function
USB Interface	H+, H-	46, 47	Out	USB Host Controller Data Output. Pins are directly connected to the USBH_P1 and USBH_N1 of the PXA270 respectively. 15K Pull-Down resistors must connected externally
	D+, D-	49, 48	In	USB Device Controller Data Output. Pins are directly connected to the USBC_N and USBC_N of the PXA270 respectively. 15K Pull-Up resistors must connected externally
Ethernet	LED_LINK	58	Out	LED activity. This pin acts as LED_RX as well as link indicator. LED_LINK is low active.
	LED_SPEED	59	Out	LED speed. This pin acts as speed indicator. It is active when the 100 Mbit signal is detected. LED_SPEED is low active.
	ETH_TX+, ETH_TX-	63, 62	Out	This pair carries the 10/100 Mbit differential transmit output. The output Manchester encoded signals have been pre-distorted to prevent overcharge on the twisted-pair media and thus reduce jitter. ETH_TX+ and ETH_TX- are fed through internal magnetics. No external magnetics required.
	ETH_RX+, ETH_RX-	61, 60	In	This input pair receives the 10/100 Mbit differential Manchester encoded data from the twisted-pair wire. ETH_RX+ and ETH_RX- are fed through internal magnetics. No external magnetics are required.

Table 6: Pin configuration of the UARTs, I²C, Timer- and PWM interface

Pin Group	Pin Name	Pin Number	Direction	Function
UART	RxD1 TxD1 CTS1 RTS1	57 56 55 54	In Out In Out	Serial Interface. The RxD1, TxD1, RTS1, and CTS1 Pins are directly connected to the BTUART of the PXA270 processor.
	RxD2 TxD2	51 50	In Out	Serial Interface. The RxD2 and TxD2 Pins are directly connected to the STUART of the PXA270 processor.
I²C Interface	SCL SDA	53 52	Out I/O	Bidirectional I²C-Interface. SCL is directly connected to GPIO117 and SDA is directly connected to GPIO118 of the PXA270 processor
Timer Interface	/TIN	1	In	Counter Input to Timer. This signal is directly connected to GPIO13 of the PXA270 processor
PWM Interface	PWM2	41	Out	PWM2 out. This signal is directly connected to GPIO11 of the PXA270 processor
	PWM3	45	Out	PWM3 out. This signal is directly connected to GPIO12 of the PXA270 processor

19 JTAG Header Pinout

Table 7: Pin configuration of the JTAG interface

Pin Group	Pin Name	Pin Number	Direction	Function
JTAG RM2mm Header	/TRST	1	In	Test Reset Pin
	TCK	3	In	Test Clock
	TDO	5	Out	Serial Output
	TDI	7	In	Serial Input
	TMS	9	In	Test Mode Select
	/RES	2	In	Reset Input
	GND	4, 6, 8, 10	Power	Ground

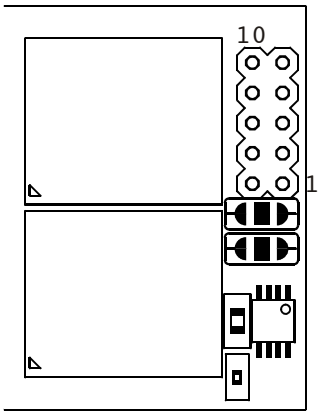

Figure 2: JTAG interface

20 DC Electrical Characteristics

Table 8: Absolute Maximum Ratings

Rating	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	-0.3	3.45	V
Output high current	$I_{OH,MAX}$		4.0	mA
Output low current	$I_{OL,MAX}$	-4.0		mA
Flash Block Write Cycles		100k		cycles
Maximum operating temperature range	T_A	0	70	°C
Storage temperature		-10	85	°C

Table 9: Recommended Operating Range

Rating	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	3.15	3.45	V
I/O voltage	V_{IO}	-0.3	3.45	V

21 Mechanical Dimensions

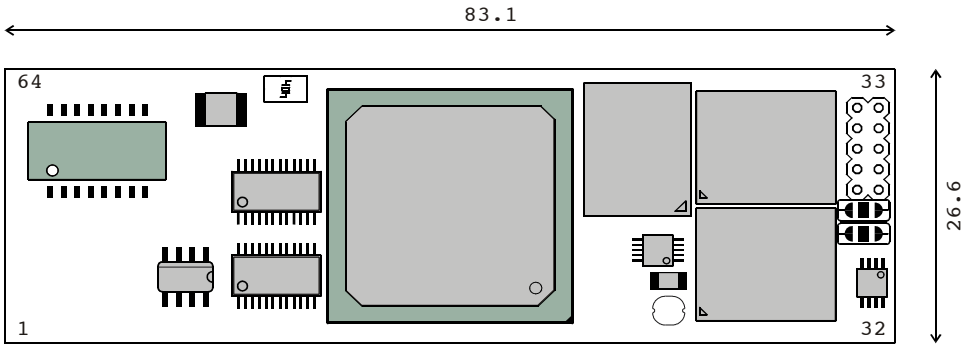

Figure 3: Mechanical Dimensions

22 Ordering Information

Ordering information for the SCB9520 socket computer boards.

Table 10: Available socket computer boards

Ordering Number	Clock	SDRAM	Flash
SCB9520-520/64/1G*	520 MHz	64 MByte	1 GByte
SCB9520-520/128/2G	520 MHz	128 MByte	2 GByte

* The SCB9520-520/64/1G is available on request. Minimum quantity is 100 pcs.

23 Life Support Applications

SCB9520 Embedded Socket Computer are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. synertronixx customers who using or selling these products for use in such applications do so at their own risk and agree to fully indemnify synertronixx for any damages resulting from such improper use or sale.

24 Contacts

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